REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV																					
PAGE																					
REV STATUS OF PAGES	**REV**																				
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12								

PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY-MM-DD 15-12-04	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, LINEAR, PRECISION, LOW POWER OPERATIONAL AMPLIFIER, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/15606**
	REV	**PAGE** 1 **OF** 12

AMSC N/A

5962-V011-16

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance precision, low power operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/15606	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	OPA2211-EP	Dual precision low power operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MO-229	Plastic quad leadless small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage ($V_S = +V_S - -V_S$) ..... 40 V maximum
Input voltage ..... $-V_S$ – 0.5 V to $+V_S$ + 0.5 V
Input current (any pin except power supply pins) ..... -10 mA to 10 mA
Output short circuit ..... Continuous 2/
Junction temperature range (T_J) ..... +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Electrostatic discharge (V_{ESD}):
Human body model (HBM) ..... ±3,000 V 3/
Charged device model (CDM) ..... ±1,000 V 4/

1.4 Recommended operating conditions. 5/

Supply voltage (V_S) ..... 4.5 V (±2.25 V) to 36 V (±18 V)
Operating temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal characteristics. 6/

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	47.3	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	51.8	°C/W
Thermal resistance, junction-to-board	θ_{JB}	21.8	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	0.7	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	21.9	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOTTOM)}$	4.2	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Short circuit to V_S / 2 (ground in symmetrical dual supply setups), one amplifier per package.
3/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
4/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
6/ For more information about traditional and new thermal metrics, see the integrated package thermal metrics application report, SPRA953.

2. APPLICABLE DOCUMENTS

AMERICAN SOCIETY OF MECHANICAL ENGINEERS (ASME)

ASME Y14.5 M - Dimensioning and Tolerancing. (DoD adopted)

(Copies of these documents are available from www.asme.org or ASME, 3 Park Avenue, New York, NY 10016.)

JEDEC Solid State Technology Association

JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155 - Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 - Recommended ESD-CDM Target Levels

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Offset voltage							
Input offset voltage	V_{OS}	V_S = ±15 V	+25°C	01		±175	µV
					±50 typical		
			-55°C to +125°C			±350	
Input offset voltage drift	$\Delta V_{OS}/\Delta T$		-55°C to +125°C	01	0.35 typical		µV/°C
Input offset voltage versus power supply	PSRR	V_S = ±2.25 V to ±18 V	+25°C	01		1	µV/V
					0.1 typical		
			-55°C to +125°C			3	
Input bias current							
Input bias current	I_B	V_{CM} = 0 V	-55°C to +125°C	01	±50 typical		nA
						±350	
Offset current	I_{OS}	V_{CM} = 0 V	-55°C to +125°C	01	±20 typical		nA
						±200	
Noise							
Input voltage noise	e_n	f = 0.1 Hz to 10 Hz	+25°C	01	80 typical		nV_{PP}
Input voltage noise density	e_n	f = 10 Hz	+25°C	01	2 typical		nV / $\sqrt{Hz}$
		f = 100 Hz			1.4 typical		
		f = 1 kHz			1.1 typical		
Input current noise density	I_n	f = 10 Hz	+25°C	01	3.2 typical		nV / $\sqrt{Hz}$
		f = 1 kHz			1.7 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Input voltage range							
Common mode voltage range	V_{CM}	$V_S \geq \pm 5$ V	+25°C	01	$-V_S + 1.8$	$+V_S - 1.4$	V
		$V_S < \pm 5$ V			$-V_S + 2$	$+V_S - 1.4$	
Common mode rejection ratio	CMRR	$V_S \geq \pm 5$ V, $-V_S + 2\ V \leq V_{CM} + V_S - 2\ V$	-55°C to +125°C	01	120 typical		dB
					114		
		$V_S < \pm 5$ V, $-V_S + 2\ V \leq V_{CM} + V_S - 2\ V$			120 typical		
					106		
Input impedance							
Differential		3/	+25°C	01	20k || 8 typical		Ω||pF
Common mode		3/	+25°C	01	10^9 || 2 typical		Ω||pF
Open loop gain							
Open loop voltage gain	A_{OL}	$-V_S + 0.6\ V \leq V_O \leq +V_S - 0.6\ V$, $R_L = 600\ \Omega$	+25°C	01	114 typical		dB
					110		
		$-V_S + 0.2\ V \leq V_O \leq +V_S - 0.2V$, $R_L = 10\ k\Omega$	-55°C to +125°C		130 typical		
					114		
		$-V_S + 0.6\ V \leq V_O \leq +V_S - 0.6\ V$, $I_O \leq 15$ mA			100		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Frequency response							
Gain bandwidth product	GBW	G = 100	+25°C	01	80 typical		MHz
		G = 1			45 typical		
Slew rate	SR		+25°C	01	27 typical		V/µs
Settling time, 0.01%	t_S	V_S = ±15 V, G = -1, 10 V step, C_L = 100 pF	+25°C	01	400 typical		ns
Settling time, 0.0015% (16 bit)	t_S	V_S = ±15 V, G = -1, 10 V step, C_L = 100 pF	+25°C	01	700 typical		ns
Overload recovery time		G = -10	+25°C	01	500 typical		ns
Total harmonic distortion + noise	THD+N	G = +1, f = 1 kHz, V_O = 3 V_{RMS}, R_L = 600 Ω	+25°C	01	0.000015 typical		%
					-136 typical		dB
Output							
Voltage output	V_{OUT}	A_{VOL} ≥ 114 dB, R_L = 10 kΩ	-55°C to +125°C	01	$-V_S$ + 0.2	$+V_S$ – 0.2	V
		A_{VOL} ≥ 110 dB, R_L = 600 Ω			$-V_S$ + 0.6	$+V_S$ – 0.6	
		A_{VOL} ≥ 100 dB, I_O < 15 mA			$-V_S$ + 0.6	$+V_S$ – 0.6	
Short circuit current	I_{SC}		+25°C	01	+30/-45 typical		mA
Open loop output impedance	Z_O	f = 1 MHz	+25°C	01	5 typical		Ω

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Power supply							
Specified voltage	V_S		+25°C	01	±2.25	±18	V
Quiescent current (per channel)	I_Q	I_{OUT} = 0 A	+25°C	01	3.6 typical		mA
						4.5	
			-55°C to +125°C			6	
Temperature range							
Operating range	T_J			01	-55	+125	°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, R_L = 10 kΩ connected to mid supply and $V_{CM} = V_{OUT}$ = mid supply.

3/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

Case X

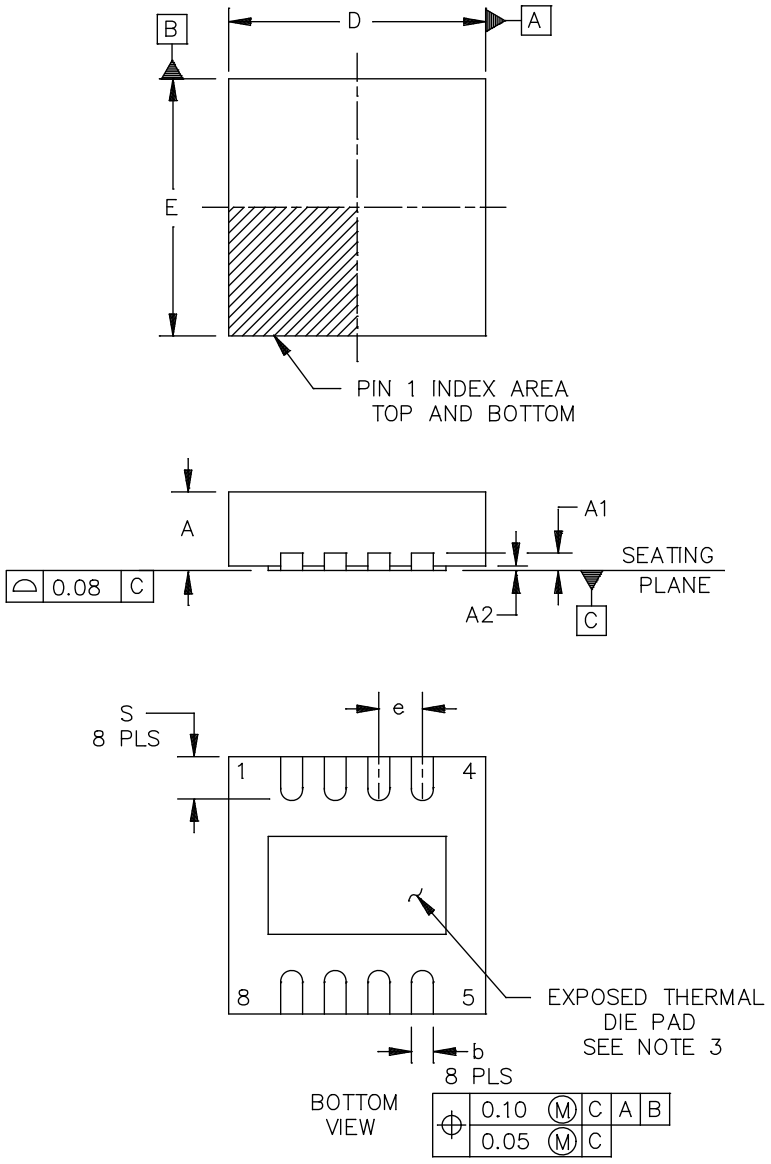

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/15606
		REV	PAGE 9

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.027	.031	0.70	0.80
A1	.000	.001	0.00	0.05
A2	.007 NOM		0.20 NOM	
b	.007	.011	0.20	0.30
e	.019 BSC		0.50 BSC	
D	.114	.122	2.90	3.10
E	.114	.122	2.90	3.10
S	.015	.023	0.40	0.60

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. The package thermal pad must be soldered to the board for thermal and mechanical performance.
4. Falls within reference to JEDEC MO-229.

FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	symbol
1	OUTPUT A
2	-INPUT A
3	+INPUT A
4	$-V_S$
5	+INPUT B
6	-INPUT B
7	OUTPUT B
8	$+V_S$

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/15606-01XE	01295	OCQM	OPA2211-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243